CLAIMS

1. A tester for testing a plurality of chips, comprising:

a source of test patterns to stimulate the plurality of chips simultaneously;

golden output signal; and

a circuit for simultaneously using outputs of the plurality of chips and said golden output signal to determine which chips pass and which chips fail, wherein said circuit is located local to said chips.

2. The tester as recited in claim 1, further comprising:

a test control device, wherein said test control device controls test patterns for testing said plurality of chips in parallel;

a checking circuit for comparing output signal of said plurality of chips with each other in response to said test patterns; and

wherein said golden output signal is used to replace defective output signal from a failing chip.

3. The tester as recited in claim 2, wherein said test control device controls a test engine.

4. The tester as recited in claim 3, wherein said test engine comprises a BIST engine.

5. The tester as recited in claim 2, wherein said test control device controls a memory with stored patterns.

6. The tester as recited in claim 2, wherein said test control device further comprises a switch for turning off signal from a chip and replacing that signal with said golden output signal.

7. The tester as recited in claim 6, wherein said switch comprises a MUX.

8. The tester as recited in claim 2, further comprising a power supply for providing a power supply voltage, wherein said test control device controls said power supply voltage to provide stress conditions to chips under test.

9. The tester as recited in claim 2, further comprising a temperature control for controlling temperature of the plurality of chips, wherein said test control device controls said temperature to provide stress conditions to chips under test.

10. The tester as recited in claim 2, wherein said checking circuit compares each chip with all other connected chips.

11. The tester as recited in claim 2, wherein said checking circuit comprises an XNOR.

12. The tester as recited in claim 11, wherein said XNOR is at least n-way, where n is the number of chips that can be tested.

13. The tester as recited in claim 12, wherein said XNOR is at least n+1-way, wherein data from a golden chip is always included in data arriving at said XNOR.

14. The tester as recited in claim 2, wherein said golden output signal is provided by a golden chip.

15. The tester as recited in claim 14, further comprising a MUX to isolate a chip and to route signal from said golden chip to replace signal from said isolated chip.

16. The tester as recited in claim 2, further comprising a visible indicator showing passing chips or failing chips.

17. The tester as recited in claim 16, wherein said visible indicator comprises a light.

18. The tester as recited in claim 2, further comprising a register for storing passing or failing chip labels.

19. The tester as recited in claim 2, further comprising sockets for holding the chips, and wherein said sockets, said test control device, said test engine, and said checking circuit are on a single card.

20. The tester as recited in claim 2, further comprising a memory for storing test results for comparison with golden test result data.

21. The tester as recited in claim 2, wherein said golden test result data are provided by a golden chip.

22. The tester as recited in claim 1, wherein said circuit comprises comparing all chip outputs with corresponding golden test result data and then combines results of all comparisons for each chip into a pass or fail signal from each chip.

23. The tester as recited in claim 21, wherein said circuit comprises an array of 2-way XNOR gates and an OR gate for each chip under test.

24. The tester as recited in claim 21, wherein said golden output signal is provided by a golden chip.

25. A device for testing integrated circuit chips comprising a test circuit for connection to a plurality of integrated circuit chips simultaneously, said test circuit for testing said integrated circuit chips during transport.

26. The device in claim 25, wherein said test circuit compares said integrated circuit chips with each other.

27. The device in claim 26, wherein said test circuit compares all said integrated circuit chips with all other integrated circuit chip that have not been found to be defective.

28. The device in claim 25, wherein said test circuit compares all said integrated circuit chips with a golden chip.

29. The device in claim 25, further comprising a power supply connected to said test circuit, wherein said power supply is for providing a power supply voltage to said test circuit and to the chips.

30. The device in claim 29, wherein said test circuit controls said power supply voltage to provide stress conditions to chips under test.

31. The device in claim 25, wherein said test circuit includes a test engine.

32. The device in claim 31, wherein said test engine comprises a BIST circuit.

33. The device in claim 31, wherein said test circuit includes a memory.

34. The device in claim 25, further comprising an indicator for identifying which of the integrated circuit chips failed said testing.

35. The device in claim 34, wherein said indicator comprises a memory.

36. The device in claim 34, wherein said indicator comprises a visual indicator.

37. A method of testing a plurality of integrated circuit chips, comprising the steps of:

a) providing a source of test patterns to stimulate the plurality of chips simultaneously;

b) providing a golden output signal; and

c) providing a circuit for simultaneously using outputs of the plurality of chips and said golden output signal to determine which chips pass and which chips fail, wherein said circuit is located local to said chips.

38. A method of testing as recited in claim 37, wherein in providing step (a) said source of test patterns comprises a BIST engine or a memory.

39. A method of testing as recited in claim 37, further comprising providing a golden chip wherein in providing step (b) said golden output signal comprises output of said golden chip, and wherein in providing step (a) providing said source of test patterns to stimulate said golden chip and the plurality of chips simultaneously.

40. A method of testing as recited in claim 37, wherein in providing step (c) said circuit uses said golden output signal to replace output signal from a chip.

41. A method of testing as recited in claim 37, wherein in providing step (c) said circuit uses said golden output signal to replace output signal from a defective chip.

42. A method of testing as recited in claim 37, wherein in providing step (c) said circuit includes a checking circuit for comparing output signal of said plurality of chips with each other in response to said test patterns.

43. A method of testing as recited in claim 37, wherein in providing step (c) said circuit includes a circuit for comparing output signals of said plurality of chips with said golden output signal to determine whether each of said plurality of chips under test passes or fails.

44. A method of testing as recited in claim 43, wherein in providing step (b) a golden chip provides said golden output signal.

45. A method of testing an integrated circuit chip, comprising the steps of:

a) providing a golden chip;

b) providing test patterns for testing the chip under test and for testing said golden chip; and

c) comparing an output signal from the chip under test with an output signal from said golden chip to determine whether the chip under test passes or fails.

46. The method of testing as recited in claim 45, wherein in providing step (b) said test patterns are provided to a plurality of chips under test simultaneously.

47. A method for testing integrated circuit chips comprising:

a) transporting said integrated circuit chips; and

b) testing said integrated circuit chips during said transporting.

48. The method in claim 47, further comprising supplying power to a test circuit connected to said integrated circuit chips during said transporting.

49. The method in claim 47, further comprising identifying ones of said integrated circuit chips which failed said testing.

50. The method in claim 49, wherein said identifying comprises storing results of said testing in a memory.

51. The method in claim 49, wherein said identifying comprises displaying a visual indicator of passing or failing chips

52. The method in claim 47, wherein said testing includes comparing output signals of said integrated circuit chips with each other.

53. The method in claim 47, wherein said testing includes comparing output signals of one integrated circuit chip with output signals of all other integrated circuit chips that have not been identified as defective.

54. The method in claim 47, wherein said testing includes comparing output signals of said integrated circuit chips with a golden chip.